In the preferred embodiment, the computer system comprises a CPU coupled through chip set or bridge logic to main memory. The bridge logic couples to a local bus such as the PCI bus. The computer system also includes a real-time expansion bus or multimedia bus for transferring real-time or multimedia data. A plurality of multimedia devices, such video devices, audio devices, MPEG encoders and/or decoders, and/or communications devices, are coupled to each of the PCI bus and the multimedia bus. In one embodiment, the multimedia bus transfers only periodic stream data, such as audio data at 44,100 samples per second, video data at 30 frames per second, or real-time communication streams at rates dependent on the transport media.

The computer system preferably includes a plurality of PCI expansion bus connector slots connected to the PCI bus for receiving add-in devices, and also preferably comprises one or more multimedia bus connector slots corresponding to respective ones of the PCI expansion bus connector slots. Thus, in one embodiment, the PCI bus and the multimedia bus are comprised on the motherboard and include respective connector slots for receiving add-in cards. Multimedia device expansion cards each include two connectors which correspond to the PCI bus and the multimedia bus. Alternatively, the multimedia devices are comprised directly on the motherboard and connect directly to the PCI bus and the multimedia bus, and connector slots are not used.

In one embodiment, the multimedia bus comprises primarily or only data lines. In this embodiment, control information for the periodic stream transfers is transferred on the PCI bus by a sourcing device, or is transferred by the CPU to the bridge logic. Thus multimedia data transfers initially involve the transfer of control or setup information on the PCI bus, or transfer of control or setup information by the CPU, to set up the transfer. This transfer of control information is followed by the transfer of the periodic data streams on the multimedia bus. Alternatively, once control/setup information has been used to set up the transfer, the periodic data stream may occupy both the PCI data lines and the multimedia bus for increased data throughput. In this embodiment, the transferring or source device transfers a multiple bus transfer request which requests simultaneous transfers on both the PCI bus and the multimedia bus. If the multiple bus transfer request is accepted, then the source device transfers data on both the PCI bus and the multimedia bus.

The present invention further includes an improved method for transferring periodic data streams on a bus in the computer system, such as periodic video streams or periodic audio streams. According to this method, the transferring device first transmits addressing and control information to set up the transfer. The transferring device then transmits a periodic transfer data request to the receiving device. The periodic transfer data request includes information regarding the frequency and amount of the periodic transfers. The receiving device determines if it can guarantee availability at the periodic time frequencies requested by the transferring device. If the receiving device indicates availability for the periodic transfers, the transferring device sets a periodic transfer flag. The transferring device then performs the periodic transfers to the receiving device at the specified time frequency. If the receiving device does not indicate availability for the periodic transfers, the transferring device performs only a single transfer and is required to transfer control information at the beginning of each subsequent periodic transfer.

In a second embodiment, the computer system includes a dedicated control channel separate from the PCI bus and the multimedia bus for transferring control information for multimedia bus data transfers. The control channel is preferably a serial bus. Alternatively, the control channel is a 4-bit, 8-bit or 16-bit bus. Thus a multimedia data transfer initially involves the transfer of control information on the dedicated control channel followed by the transfer of the periodic data streams on the multimedia bus.

In a third embodiment, the multimedia bus comprises separate channels for different data types. In the preferred embodiment, the computer system includes a first video data channel for transferring video and/or graphics information, a second audio channel for transferring audio information, and optionally a third channel for transferring communications information. The video channel is preferably 32 bits, 24 bits, or 16 bits. Alternatively, the video channel is an 8-bit bus or a very high speed serial bus. The audio channel is preferably 16 bits or 8 bits. Alternatively, the audio channel is also a 32-bit bus or a very high speed serial bus. The communications channel is also preferably either 16 or 8 bits. This third embodiment may use the PCI bus for control information transfers, or may use a separate control channel separate from the PCI bus and the multimedia bus for transferring control information for the periodic stream transfers.

In a fourth embodiment, each multimedia device has a high speed link directly to system memory, which is preferably single or multiple ported memory. These individual links are preferably high speed serial interconnects but, alternatively, may be 4-bit, 8-bit, 16-bit, 24-bit, 32-bit, 64-bit or any combination thereof In this embodiment, intelligent buffering is preferably implemented within the core logic, and arbitration for access to main memory is preferably implemented within the core logic. Each of the multimedia devices uses its dedicated memory data channel to perform data accesses and transfers directly to the main memory, bypassing PCI bus arbitration and PCI bus cycles. Alternatively, each of the multimedia devices includes a high speed memory channel directly to the memory controller in the core logic for accessing system memory.

In a fifth embodiment, the multimedia bus is time sliced wherein time slices or time slots are allocated in proportion to the required bandwidth. In one embodiment, the time slices are each a constant size and a number of the equal sized time slots are allocated to respective data streams in proportion to the required bandwidth. In this embodiment, for example, video data streams may be allocated more time slots than audio data streams because of the increased data transfer band width requirements of video streams. Alternatively, the time slots are not equally sized, but rather are dynamically sized or allocated to data streams in proportion to the required bandwidth.

In a sixth embodiment, multimedia devices that connect to the multimedia bus include intelligent controller circuitry which includes knowledge of the respective time slice allocated to the multimedia device. In this embodiment, arbitration for the multimedia bus is not required. Rather, a multimedia device which is a transmitter of video data monitors the bus and includes controller circuitry which begins transmitting the video data when the device's respective time slot occurs. A corresponding receiver device also knows that the current time slot is a video time slot and monitors the bus to receive the data.

In this embodiment, the interface circuitry of each of the multimedia devices are programmed at boot time for a static allocation of time slots. Alternatively, the interface circuitry in the multimedia devices is dynamically programmed by a